CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters PATENT is:

1. A silicon-on-insulator (SOI) metal oxide field effect transistor (MOSFET) device comprising:

an implanted back-gate region located atop an oxide layer, wherein a surface portion of said implanted back-gate region includes a back-gate oxide formed thereon;

a body region located atop said back-gate oxide;

a gate dielectric located atop a surface portion of said body region; and

a polysilicon gate located atop a portion of said gate dielectric.

2. The SOI MOSFET of Claim 1 further comprising back-gate-STI regions located under portions of said body region.

3. The SOI MOSFET device of Claim 1 wherein said body region further includes source/drain regions and source/drain extension regions.

4. The SOI MOSFET device of Claim 1 wherein said polysilicon gate includes spacers on sidewalls thereof.

5. The SOI MOSFET device of Claim 1 further comprising raised source/drain regions located atop a portion of said body region.

6. The SOI MOSFET device of Claim 1 further comprising silicide regions located atop a portion of said body region and atop the polysilicon gate.

7. The SOI MOSFET device of Claim 1 further comprising a dielectric material encapsulating said polysilicon gate.

8. The SOI MOSFET device of Claim 7 wherein said dielectric material includes conductive filled contact holes.

9. The SOI MOSFET device of Claim 1 wherein said implanted back-gate serves as a threshold control system for the polysilicon gate.

10. A method of fabricating a silicon-on-insulator (SOI) metal oxide field effect transistor (MOSFET) device comprising the steps of:

providing a structure including at least a back-gate oxide located atop a Si-containing layer, said Si-containing layer is a component of a SOI wafer;

forming alternating regions of back-gate-STI and first polysilicon atop said back-gate oxide;

forming a second polysilicon layer atop said alternating regions of back-gate-STI and first polysilicon;

implanting a back-gate region into said polysilicon layers;

forming an oxide layer on said second polysilicon layer;

bonding a holding-substrate wafer to said oxide layer and flipping the bonded structure to expose layers of said SOI wafer;

removing selective layers of said SOI wafer stopping on said Si-containing layer;

converting a portion of said Si-containing layer into a body region; and

forming a gate dielectric and a polysilicon gate atop said body region.

11. The method of Claim 10 further comprising forming raised source/drain regions atop said body region that lays adjacent to said polysilicon gate.

12. The method of Claim 11 further comprising converting said raised source/drain regions into silicide regions.

13. The method of Claim 10 wherein said bonding is performed at a temperature of about 900°C to about 1100°C for a time period of from about 1.5 hours to about 2.5 hours.

14. The method of Claim 10 wherein said bonding is performed at a temperature of from about 18°C to about 27°C in an inert ambient.

15. The method of Claim 10 wherein said body region is formed by a masked ion implantation process.

16. The method of Claim 10 wherein said alternating polysilicon region have under-cut sidewalls.

17. The method of Claim 10 further comprising encapsulating said polysilicon gate with a dielectric material, said dielectric material having conductively filled contact holes abutting said polysilicon gate.